PRINTER RUSH
(PTO ASSISTANCE)

Application : 10/089,650 **Examiner :** S.T. Baderman **GAU :** 2113

From: S. Winslow **Location:** (IDC) FMF FDC **Date:** 12-15-05

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DOC CODE	DOC DATE	MISCELLANEOUS
☐ 1449		☐ Continuing Data
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☐ OATH		
☐ 312		
☐ SPEC		

[RUSH] **MESSAGE:** Pages 7, 8, 14 & 15 have incomplete sentences

Please advise

Thanks

[XRUSH] **RESPONSE:** See misc comm

Done

INITIALS: RK

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REV 10/04

Attorney's Docket No.: 12816-046US1
Client's Ref. No.: S1699 GC/sta

OFFICIAL COMMUNICATION FACSIMILE:

OFFICIAL FAX NO: (703) 308-6642

Number of pages including this page 7

Attention: Rori Burch, USPTO Publishing Division

Applicant : Andreas Pechlaner et al.
Serial No. : 10/089,650
Filed : August 14, 2002

Art Unit : 2114
Examiner : Scott T. Baderman

Title : Protection circuit for an access-arbitrated bus system network

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attached to this facsimile communication cover sheet is Response to Notice to File Corrected Application papers, faxed this 24th day of January, 2006, to the United States Patent and Trademark Office.

Respectfully submitted,

Date: January 24, 2006

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Attorney's Docket No.: 12816-046US1 / S1699 GC/sta

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Andreas Pechlaner et al.	Art Unit	: 2114
Serial No.	: 10/089,650	Examiner	: Scott T. Baderman
Filed	: August 14, 2002		
Title	: PROTECTION CIRCUIT FOR AN ACCESS-ARBITRATED BUS SYSTEM NETWORK		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

Responsive to the Notice to File Corrected Application Papers mailed December 29, 2005 (a copy of which is enclosed), applicant as a large entity submits herewith the following:

☒ Specification pages 7, 8, 14, and 15.

No new matter has been added.

It is understood that this perfects the application and no additional papers or filing fees are required.

Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 1/24/06

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CERTIFICATE OF TRANSMISSION BY FACSIMILE

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January 24, 2006
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Iria Zarembok
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UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Serial Number
10089650

Date Mailed
12/29/05

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given 30 days from the mail date of this Notice within which to correct the informalities indicated below. A failure to reply will result in the application being ABANDONED. This period for reply is NOT extendable under 37 CFR 1.136 (a) or (b).

- Specification pages 7, 8, 14 and 15 have data missing due to an incomplete amendment. Fax missing information to number below or e-mail.
    - For status updates visit http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR System, contact the Electronic Business Center (EBC) toll free at 866-217-9197.

APPLICANT MUST SUPPLY MISSING INFORMATION WITHIN 30 DAYS OF THE MAIL DATE OF THIS NOTICE.

A copy of this notice MUST be returned with the reply. Please address response to Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

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figure 4 shows the isolation device for isolating the network sections in the second embodiment of the inventive protective circuit, shown in figure 3.

Figure 2 shows a CAN bus system network with a first embodiment of the inventive protective circuit.

As can be seen in figure 2, the CAN bus system network comprises two CAN bus lines, namely a high level CAN bus line 1a, 1b (CAN-H) and a low level CAN bus line 2a, 2b (CAN-L). In the example shown in figure 2, the overall bus system network has three CAN control nodes 3, 4, 5. Each of the three control nodes 3, 4, 5 has a respective transceiver 3a, 4a, 5a and a microprocessor 3b, 4b, 5b. The transceivers 3a, 4a, 5a respectively comprise a transceiver transmitter and a transceiver receiver, with the transceiver transmitter being connected to the microprocessor via a respective transmission line 3c, 4c, 5c, and the transceiver receiver being connected to the microprocessor via a line 3d, 4d, 5d. The CAN bus lines 1a, 2a, 1b, 2b are connected to the control node 3 via control node connecting lines 6, 7, to the control node 4 via connecting lines 8, 9 and to the control node 5 via connecting lines 10, 11.

Connected into the CAN bus lines 1a, 1b, 2a, 2b is an inventive protective circuit 12 for the CAN bus system network on the basis of a first embodiment. The interposition of the protective circuit 12 in the overall bus system network subdivides said network into two network sections in the example shown in figure 2. The first network section comprises the control node 3, the connecting lines 6, 7 for the control node 3 and the CAN bus lines 1a, 2a, to which bus line connections 13a, 14a for the inventive protective circuit 12 are connected. The second network section is formed by the two CAN control nodes 4, 5, which are connected to the CAN bus lines 1b, 2b via connecting lines 8, 9 and 10,

11. The CAN bus lines 1b, 2b are connected to CAN bus line connections 13b, 14b for the inventive protective circuit 12.

In the inventive protective circuit 12 based on the first embodiment, the fault recognition device has a first fault state detection circuit 15 for detecting a fault state in the first network section and a second fault state detection circuit 16 for detecting a fault state in the second network section. The outputs of the two fault state detection circuits 15, 16 are connected to a fault recognition logic circuit 19 via lines 17, 18. When a fault state is detected in one of the two network sections by one of the two fault state detection circuits 15, 16, the fault recognition logic circuit 19 outputs a control signal via a control switching line 20 to a switching device 21 for the purpose of switching internal bus lines 1c, 2c within the protective circuit 12, the internal bus lines 1c, 2c respectively connecting the bus line connections 14a, 14b and 13a, 13b to one another. The switching device 21 has a plurality of switches 22, 23 connected in parallel, with a respective switch being provided for each bus line 1c, 2c. The switches 22, 23 are preferably semiconductor switches which block in both signal directions in the off state. The semiconductor switches preferably comprise two reverse-connected series MOSFET transistors whose forward resistance is less than 10 Ω.

The fault state detection circuits 15, 16 detect short circuits between the lines in a network section, for example between the connecting lines 6, 7 for the control node 3 in the first network section, as a first fault state.

In the example shown in figure 2, the first network section can be a network section which is arranged in

If, conversely, the second network section B is transmitting, the logic isolation circuit 29 receives a logically dominant 0 signal via the circuit 28 and forwards it on the line 30 to the first network section A via the transceiver 25. From the operating situations B4, B5, B6, the two network sections A, B are isolated by logic such that no dominant logic low level data transmission signals are connected by the isolation circuit 29, but instead a blocking signal is inevitably produced. In this case, the signal outputs 44, 49 of the two transmission multiplexers 35, 34 are set to the recessive high level data transmission signal.

The table below shows the transmitted and received signals in a control node 3 in the first network section A and a control node 4 in a second network section B for the various operating situations B.

The control node 3 transmits a transmitted signal S_1 and receives a received signal E_1. The control node 4 transmits a transmitted signal S_2 and receives a received signal E_2.

Operating situation B	S_1	S_2	E_1	E_2
B1 Quiescent state	1	1	1	1
B2 Transmitter in network section A	0	1	0	0
B3 Transmitter in network section B	1	0	0	0
B4 Transmitter in both network sections	0	0	0	0
B5 Fault in network section A	x	0/1	x	S_2
B6 Fault in network section B	0/1	x	S_1	x

Table 2

In one preferred development of the logic isolation circuit 29 shown in figure 4, the signal input 42 of the transmission multiplexer 35 is connected to the signal output 40 of the reception multiplexer 32 with DC decoupling. In addition, the first signal input 47

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of the transmission multiplexer 34 and the signal output 45 of the reception multiplexer 33 are connected with DC decoupling. In this case, the connecting lines 41, 46 are preferably DC-decoupled by interposed optocouplers. The DC isolation of the two network sections by the optocouplers has the particular advantage that the various network sections can be provided with different supply voltages V_{BB} for the bus lines.

The logic isolation circuit 29 is connected to the control nodes 3, 4, 5 via a fault bus line 24 in order to transmit information data.

As can be seen from figure 2 and figure 3, both embodiments of the inventive protective circuit are of symmetrical design, which means that the inventive protective circuit 12 can be used in bus lines 1, 2, with the bus line connection 14a being able to be interchanged with the bus line connection 14b, and the bus line connection 13a being able to be interchanged with the bus line connection 13b. Preferably, the bus line connections 13a, 14a and the bus line connections 13b, 14b can also be interchanged when the protective circuit 12 is inserted into the bus system network. This affords the particular advantage of simple assembly.

The inventive protective circuit 12 is distinguished by very low circuit complexity, which facilitates its design using standard chips. The inventive protective circuit can be used universally in all access arbitrated bus system networks, such as a CAN bus system, a J 1850 bus system or a CSMA bus system. It can be interposed at any points within the bus system network. The direct monitoring of the physical level state on the bus lines means that the inventive